

PRELIMINARY AMENDMENT

Serial Number: Unknown

Filing Date: Herewith

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

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56. (New) The circuit of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (New) The circuit of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

58. (New) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

59. (New) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

60. (New) The circuit of claim 55, wherein the top layer includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the first dielectric layer.

61. (New) The circuit of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

62. (New) A circuit on a single substrate, comprising:
a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

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63. (New) The circuit of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. (New) The circuit of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

65. (New) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

66. (New) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

67. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer

including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si_3N_4) top layer which exhibits a high resistance to oxidation at

high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

68. (New) The circuit of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (New) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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70. (New) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (New) The circuit of claim 67, wherein the silicon nitride (Si_3N_4) top layer includes a silicon nitride (Si_3N_4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (New) The circuit of claim 67, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

73. (New) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si_3N_4) top layer of approximately a third of the first thickness

which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness of less than 12 nanometers (nm).

74. (New) The structure of claim 73, wherein the top layer exhibits a high resistance to boron

75. (New) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (New) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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77. (New) A circuit on a single substrate formed by the method comprising:
- forming a logic device including a first transistor and a memory device including a second transistor on a single substrate;
 - forming a pair of gate oxides on the first transistor and the second transistor to a first thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;
 - forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and
 - forming the other of the pair of gate oxides to a second thickness.